REMARKS

Claims 1, 3, 4, 7, 17, 19, 20, 23, 33, 35, 36 and 39 have been amended. Non-elected claims 10-16, 26-32 and 42-48 have been canceled without prejudice. Claims 1-9, 17-25, 33-41 and 49-53 are now pending in this application.

Claims 1-9, 17-25, and 33-41 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicant traverses the rejection. The term "storage node" is often used in the art of imager pixel circuits as being a point in the pixel circuit where a charge or voltage is stored. Nevertheless, in order to expedite prosecution of the application, claims 1, 3, 4, 7, 17, 19, 20, 23, 33, 35, 36 and 39 have been amended to recite "circuit" instead of "node." Claims 1-9, 17-25 and 33-41 are in full compliance with § 112.

Claims 1-9, 17-25, 33-41, and 49-53 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Yadid-Pecht et al., U.S. Patent No. 6,515,702 ("Yadid-Pecht"). This rejection is respectfully traversed.

Yadid-Pecht does not disclose the subject matter of independent claims 1, 17 and 33. Specifically, Yadid-Pecht does not disclose or suggest an active pixel sensor or an imager device having a plurality of pixels where "<u>each of said pixels</u>" comprises "a first storage circuit" and a "second storage circuit," as defined by claims 1, 17 and 33. [Emphasis added.]

Similarly, with regard to claim 49, Yadid-Pecht does not disclose or suggest a method for operating an active pixel sensor, the method comprising "storing a reset voltage of [a] photosensitive element <u>within [a] pixel</u>," and "storing <u>within said pixel</u> a voltage level of said photosensitive element after [an] integration period." [Emphasis added.]

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With regard to claim 53, Yadid-Pecht also does not disclose or suggest an active pixel sensor having a plurality of pixels, wherein "each of said pixels" comprises "at least one sample and hold circuit for storing at least one of a reset voltage and a voltage level of a photosensitive element after an integration period." [Emphasis added.]

As acknowledged in the Office Action, Yadid-Pecht, to the contrary, discloses that the first and second storage circuits are located in a "readout circuit 70" that is separate from the pixel. See Office Action at 3-4, see also Yadid-Pecht at FIG. 3. This is also evident from the row select transistor 60 of FIG. 3 of Yadid-Pecht, which must be activated in order to transfer the reset and integration voltages to the separate storage circuits in the double sampling circuit 70.

At least for the reasons mentioned above, claims 1, 17, 33, 49 and 53 are allowable over Yadid-Pecht.

Claims 2-9, 18-25, 34-41 and 50-52 depend from claims 1, 17, 33 and 49, and are also allowable at least for the reasons provided above with regard to claims 1, 17, 33 and 49, and also because Yadid-Pecht fails to teach or suggest the respective inventive combinations defined by claims 2-9, 18-25, 34-41 and 50-52.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejections and to pass this application to issue.

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Respectfully submitted,

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